Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **INPUT**
2. **OUTPUT**
3. **OUTPUT**
4. **ADJUSTMENT**
5. **INPUT**
6. **OUTPUT**

**.088”**

**2**

**3**

**4**

**1**

**5 6**

**MASK**

**REF**

**.074”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .006” min**

**Backside Potential: Output**

**Mask Ref: LMH317D**

**APPROVED BY: DK DIE SIZE .074” X .088” DATE: 11/27/17**

**MFG: NATIONAL THICKNESS .010” P/N: LM317K**

**DG 10.1.2**

#### Rev B, 7/1